UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,899	09/09/2003	Christian Peters	P2001,0182	5645

24131 7590 05/10/2006

LERNER GREENBERG STEMER LLP
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,899	PETERS, CHRISTIAN	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by US 6215135 to Schröder.

Regarding claim 1, Schröder discloses a thyristor structure in fig. 1, comprising: a first terminal d5 formed as a first region having a first conductivity type (P), fig. 1, column 2 line 44; a second region WLL of a second conductivity type (N), col. 2 line 41, adjoining said first region d5; a third region SBSTR of the first conductivity type (P), col. 2 line 39, adjoining said second region WLL and having a common surface (top surface) with said second region WLL; a second terminal d2 functioning as a fourth region formed of the second conductivity type (N), col. 2 line 46, and adjoining said third region SBSTR; said first terminal d5 and second terminal d2 each being connected to a respective one of a first potential V_{DD} and a second potential V_{SS}, fig. 1; auxiliary electrodes G2/g1, fig. 1, disposed on said common surface and each adjoining one of said second and third regions WLL/SBSTR; said auxiliary electrodes g2/g1 being

formed as gate electrodes, fig. 1, said auxiliary electrode g2/g1 being electrically conductively connected with a respective one of said first terminal d5 and said second terminal d2, and said auxiliary electrodes g2/g1 being so formed on said common surface (top surface) that no parasitic effect between said first terminal d5 and said second terminal d2 leads to a conductive state between said two terminals, fig. 2; and a control terminal d3, fig. 1, for controlling the thyristor structure by an applied current embodied in one of said second region WLL and said third region SBSTR, fig. 1, said control terminal d3 being formed of the same conductivity type (P) as a surrounding region thereof (SBSTR).

In the recitation 'for thyristor' that has not been given patentable weight because it have been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951).

With respect to 'no parasitic effect between said first terminal and said second terminal leads to a conductive state between said two terminals', Schröder discloses the structure that is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

3. Claims 1, 3 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5739998 to Wada.

Regarding claim 1, Wada discloses a thyristor structure in fig. 11, comprising: a first terminal 81, column 6 line 53, formed as a first region 81 having a first conductivity type (P), fig. 8; a second region 83, column 6 line 48, of a second conductivity type (N) adjoining said first region 81; a third region P-well (middle), fig. 8, of the first conductivity type (P) adjoining said second region 83 and having a common surface with said second region 83 (top surface of substrate P); a second terminal N^+ (in middle P-well, gate 3C) functioning as a fourth region formed of the second conductivity type (N), and adjoining said third region P-well; said first terminal 81 and second terminal N^+ each being connected to a respective one of a first potential V_{DD} and a second potential V_{dd}, fig. 8; auxiliary electrodes 3A/3C, fig. 8, disposed on said common surface and each adjoining one of said second and third regions 83/P-well; said auxiliary electrodes 3A/3C being formed as gate electrodes, fig. 8, said auxiliary electrode 3A/3C being electrically conductively connected with a respective one of said first terminal 81 and said second terminal N^+, and said auxiliary electrodes 3A/3C being so formed on said common surface (top surface of substrate P) that no parasitic effect between said first terminal 81 and said second terminal N^+ leads to a conductive state between said two terminals, fig. 6-8; and a control terminal P^+ (in P-well connects to Vss), fig. 8, for controlling the thyristor structure by an applied current embodied in one of said second region 83 and said third region p-well, fig. 8, said control terminal P^+ being formed of the same conductivity type as a surrounding region thereof (P-well region).

Regarding claims 3, 6, Wada discloses an over voltage protection configuration in fig. 8, comprising: a thyristor structure containing; a first terminal 81 formed as a first

region 81 having a first conductivity type (P); a second region 83 of a second conductivity type (N) adjoining a first region 81, a third region P-well of the first conductivity type (P) adjoining said second region 83 and having a common surface with said second region 83, fig. 8, a second terminal N^+ (in P-well) functioning as a fourth region formed of the second conductivity type (N), a component 2 to be protected , fig. 6, disposed in an electrically conductive manner between said first terminal 81 and said second terminal N^+; said first terminal 81 and second terminal N^+ each being connected to a respective one of a first potential V_{DD} and a second potential V_{DD}, fig. 8, auxiliary electrodes 3A/3C disposed on said common surface and each adjoining one of said second and third regions 83/P-well; said auxiliary electrodes 3A/3C being formed as gate electrodes 3A/3C, said auxiliary electrodes being electrically conductively connected with a respective one of said first terminal 81 and said second terminal N^+, said auxiliary electrode 3A/3C being so formed on common surface that no parasitic effect between said first terminal 81 and said second terminal N^+ leads to a conductive state between said two terminals; and a control terminal P^+ (in P-well connected to Vdd), fig. 8, for controlling the thyristor structure by an applied current, embodied in one of said second region 83 and said third region P-well; and an over voltage detector 1 connected to and detecting an over voltage across the component 2 to be protected, fig. 6, said control terminal P^+ being formed of the same conductivity type as a surrounding region thereof (P-well region).

In the recitation 'for thyristor' that has not been given patentable weight because it have been held that a preamble is denied the effect of a limitation

where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951).

With respect to 'no parasitic effect between said first terminal 81 and said second terminal leads to a conductive state between said two terminals', Wada discloses the structure that is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5739998 to Wada et al. in view of US 4695916 to Satoh et al.

Regarding claims 2 and 4, Wada discloses the thyristor structure according to claim 1, wherein said auxiliary electrodes 13A/13C are each formed from a conventional MOS type FET, column 1 line 19-20.

But Wanda does not discloses the thyristor structure wherein said auxiliary electrodes are each formed from a conductive region made of

polysilicon and an auxiliary oxide insulating, said conductive region from said common surface. Such conductive polysilicon and gate oxide are typical materials used in MOS FET construction; see Ishizaka in column 18 line 64-65, fig. 17.

Regarding claim 5, Wada does not discloses the over voltage protection configuration, wherein a supply voltage of the component to be protected is connected to said first terminal and to said second terminal.

However, Satoh reference discloses the over voltage protection configuration in fig. 9 wherein a supply voltage of the component 11 to be protected is connected to said first terminal 12 and to said second terminal 13. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the parallel connection of the thyristor and the protecting component teaching of Satoh with Wada's device, because it would have prevented the generation of a traverse mode voltage as taught by Satoh, column 5 line 50-55.

Response to Arguments

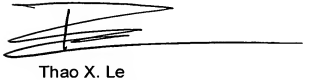
6. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
08 May 2006